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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,963	11/10/2003	Darrell Rinerson	UNTP023	2962
42958	7590	12/21/2004	EXAMINER	
UNITY SEMICONDUCTOR CORPORATION			LE, THAO P	
250 NORTH WOLFE ROAD			ART UNIT	
SUNNYVALE, CA 94085			PAPER NUMBER	
			2818	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/605,963

Applicant(s)

RINERSON ET AL.

Examiner

Thao P. Le

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) 17-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>1 page</u> . | 6) <input type="checkbox"/> Other: _____  |

DETAILED ACTION

***Election/Restriction***

1. Examiner confirms that Applicants elected to prosecute Claims 1-16 and have withdrawn Claims 17-22 without prejudice.

***Information Disclosure Statement***

2. Information Disclosure Statement (IDS) filed on **02/23/04** and made of record.  
The references cited on the PTOL 1449 form have been considered.

**Claim Rejections**

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7-8 are rejected under 35 USC 102 (b) as being anticipated by  
Bailey, U.S. Patent No. 6,249,104.

Regarding claim 1, Bailey discloses a conductive memory device comprising  
(See Fig. 10B and corresponding Cols.):

- . a bottom electrode 1178 having a top face with a first surface area;
- . a top electrode 1182 located above the bottom electrode having a bottom face with a second surface area;
- . a multi-resistive state element 1180 sandwiched between the bottom electrode and the top electrode and having a bottom face with a third surface area and a top face with a fourth surface area, the multi-resistive state element's bottom face being in contact with the bottom electrode's top face, and the multi-resistive state element's top face being in contact with the top electrode's bottom face;
- . wherein the fourth surface area is not equal to the second surface area (Fig. 10B).

Regarding claim 2, Bailey discloses the device in claim 1 and further discloses a diffusion barrier layer 1186 and the barrier layer covers the sidewalls of the bottom electrode, top electrode, and the multi-resistive state element (Fig. 10B).

Regarding claims 3-4, Bailey discloses the diffusion barrier is also an etch stop and made of Silicon Nitride (lines 28-31, Col. 13).

Regarding claim 7, Bailey discloses a sidewall layer 1186 and the sidewall layer covers the sides of bottom electrode, top electrode, and the multi-resistive state element.

Regarding claim 8, Bailey discloses wherein the second surface area is smaller than the fourth surface area (Fig. 10B).

5. Claims 1, 5-6 are rejected under 35 USC 102 (e) as being anticipated by Kato, U.S. Patent No. 6,809,360.

Regarding claim 1, Kato discloses a conductive memory device comprising (See Figs. 1D-1J and corresponding Cols.):

- . a bottom electrode 14 having a top face with a first surface area;
- . a top electrode 16 located above the bottom electrode having a bottom face with a second surface area;
- . a multi-resistive state element 15 sandwiched between the bottom electrode and the top electrode and having a bottom face with a third surface area and a top face with a fourth surface area, the multi-resistive state element's bottom face being in contact with the bottom electrode's top face, and the multi-resistive state element's top face being in contact with the top electrode's bottom face;
- . wherein the fourth surface area is not equal to the second surface area (Fig. 1F).

Regarding claims 5-6, Kato discloses the device in claim 1 above and further discloses wherein the first surface area is larger than the third surface area and wherein the second surface area is larger than the fourth surface area (See Fig. 1 drawings).

#### **Claim Rejections - 35 USC § 103**

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 9-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey, U.S. Patent No. 6,249,104.

Regarding to claims 9-14, Bailey discloses the device as claimed in claims 1, 8 but fails to disclose the device further including a hard mask layer formed on the top electrode and a spacer formed on the sides of the top electrode and wherein the spacer material is dielectric which selected from silicon nitride, silicon oxide, titanium oxide, SiON or AlO. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to form a hard mask on the top electrode and a spacer on the sides of the top electrode in order to protect the top electrode from etching and to prevent the leakage current. It is well known in the art that dielectric materials such as silicon nitride, silicon oxide, titanium oxide, SiON or AlO are used as spacer to prevent leakage current.

Regarding claim 15, Bailey discloses the bottom electrode, the top electrode, and the state element each have sides and these sides are cover by a sidewall layer (hydrogen barrier layer, Fig. 10B).

Regarding claim 16, it is obvious that the top, bottom, and multi-resistive state element lie in the X-Y plane and the direction of current conduction through the conductive memory device is parallel to the Z-axis.

8. Other references listed in PTO-892 form also disclose a similar device to present invention.

9. When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao P. Le whose telephone number is 571-272-1785. The examiner can normally be reached on M-T (7-6).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thao P. Le  
Examiner  
Art Unit 2818